IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

A New Topology of Hybrid Multilevel Inverter

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Abstract

This paper introduces a modified multilevel inverter topology that has many steps with fewer power electronic switches. The proposed circuit consist of bypassed–diode technique. The optimal structures of this topology are investigated for various objectives, such as minimum number of switches, diodes, total harmonic distortion and minimum standing voltages on the switches for producing the maximum output voltage steps. This new topology use only eight switches, four diodes for the design of 31-level inverter. The working of this multilevel inverter has been studied using both resistive and inductive loads. Validation is provided by conducting simulation studies on a induction motor drive.

Introduction

MULTILEVEL inverter have drawn much attention in medium-high voltage and high-power applications in recent years. The most popular advantage of the multilevel inverter compared with traditional voltage source inverter are high-power quality waveforms with lower distortion and a low blocking voltage by switching devices. As the number of level increased, these advantage will be enhanced[1]. There are three basic kinds of multilevel inverter topologies; the neutral point clamped(NPC) inverter, the flying-capacitor(FC) inverter, and the cascaded H-bridge (CHB)multi-level inverter[2]. The NPC multilevel inverter also called diode-clamped can be considered the first generation of multilevel inverter, the FC multilevel inverter offers some redundant switching states. However, the control scheme becomes complicated. Moreover, the number of capacitors increases by increasing the number of voltage levels.

The CHB multilevel inverters use series-connected H-bridge cells with an isolated dc voltage sources connected to each cell[3]. The CHB multilevel inverters can be divided into two groups from the values of the dc voltage sources, the symmetric and the asymmertric topology[4]. In the symmetric topology, the values of all of the dc voltage sources are equal. This characteristics give the topology good modularity. However, the number of switching devices rapidly increases by increasing the number of output voltage level. In order to increase the number of output voltage level, the value of the dc voltage sources are selected to be different these topologies are called asymmetric. The topologies discussed above, are the conventional topologies. Many other multilevel inverter topologies have been introduced in recent years[5]. One of the topologies is the modular multilevel inverter. This paper produces a new multilevel inverter topology using bypassed-diode technique. The proposed multilevel inverter uses reduced number of switches. Initially , the proposed bypassed-diode is described and then the basic H-bridge structure is discussed. The optimal structure of the proposed multilevel inverter regarding several factors(e.g. number of switches, standing voltage on each switch, THD, harmonics etc) are also obtained. The proposed multilevel inverter is compared with other multilevel inverter topologies considering the number of switches. A design example is given for both single and three phase system and the performance of the inverter is studied using MATLAB/SIMULINK

Suggested Topology

A *Proposed Bypassed-diode Technique*

The basic unit for multilevel inverters, which is recommended in [6] and [7], is illustrated in Fig. 1(a) and in 1(b).

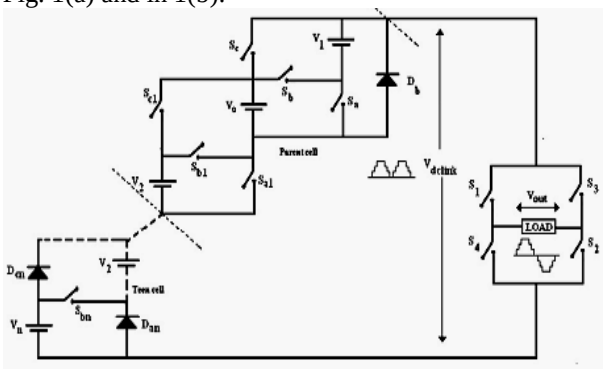

Fig 1(a) Basic unit suggested in[6]

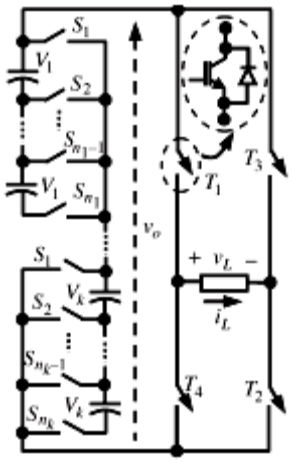

Fig 1(b) Basic unit suggested in[7]

The proposed inverter employing bypassed-diode technique. As depicted in Fig. 2(b), the topology consists of n dc voltage sources. In general, the dc voltage source can have different values. However, in order to have equal voltage steps they are considered to be the same and equal to V_{dc}. Each unit of the inverter consist of one switch, diode and a dc voltage source. The switch S_1, S_2, S_3, S_4 are unidirectional switches which are connected in series with the dc voltage source and parallel with the bypassed diode D_1 , D_2 , D_3, D_4. In this proposed topology equal number of switches and diode are required for each voltage sources.

The proposed multilevel inverter can only generate zero and positive voltage levels which is shown in fig 2(a). The zero output voltage level is obtained when all switches are turned OFF. The other voltage levels are generated by proper switching between the switches.

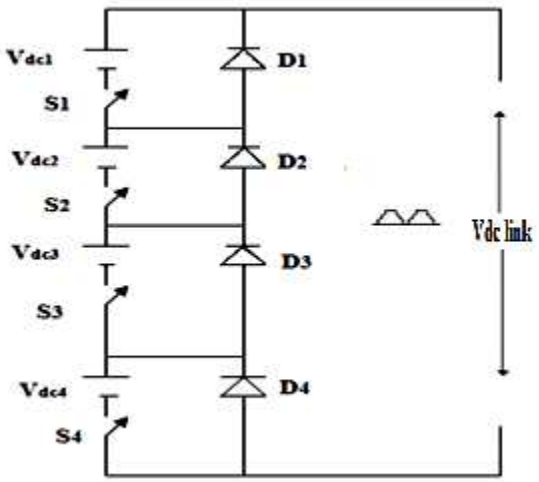

Fig 2(a) Proposed bypassed diode technique

B Proposed Generalized Multilevel Inverter

The proposed multilevel inverter use bypassed diode technique to achieve the desired voltage and number of voltage levels. The output voltage of the main inverter is always positive or zero. To operate as an inverter, it is necessary to change the voltage polarity in every half cycle. For this purpose, an H-bridge inverter is added to the output of the main inverter.

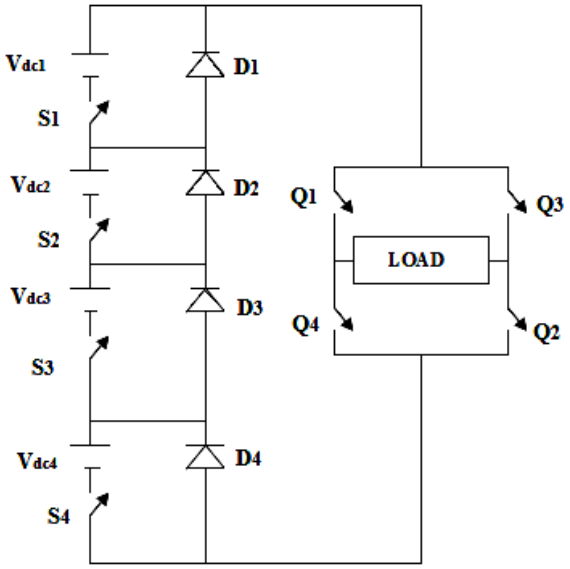

Fig 2(b) proposed inverter topology

It is important to note that the switches of the H-bridge must withstand higher voltage. However, these switches is turned on and off once a fundamental cycle. So, these switches would be high voltage low frequency switches. The switch Q_1, Q_2 will conduct for positive cycle and Q_3 and Q_4 for negative half cycle, the sample waveform is shown in fig 3,

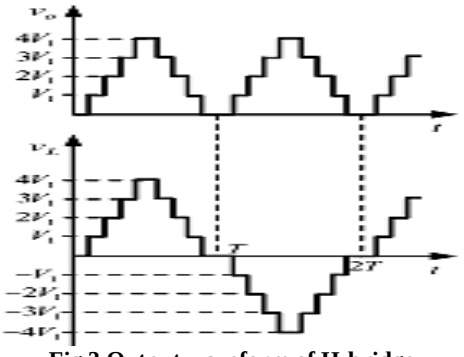

Fig 3 Output waveform of H-bridge

The S number of dc source or stages and the associated number output level can be calculated by using the equation

$$N_{level} = 2^{s+1} - 1 \qquad (1)$$

For example if S=3, the output wave form has 15 levels.

Voltage on each stage can be calculated by using the equation

$$V = 2^{s-1}.V_{dc} \quad (2)$$

The number of switches used in this topology is given by the equation

$$N_{switch} = S + 4 \quad (3)$$

TABLE

Values of V_{out} for different state of switches

S. No	State	ON Switch	Current Flow Path	Voltage Levels
1	I	S_1	$S_1D_4D_3D_2$	+1Vs
2	II	S_2	$S_2D_1D_4D_3$	+2Vs
3	III	S_1S_2	$S_1S_2D_4D_3$	+3Vs
4	IV	S_3	$S_3D_1D_2D_4$	+4Vs
5	V	S_1S_3	$S_1D_4S_3D_2$	+5Vs
6	VI	S_2S_3	$S_2S_3D_1D_4$	+6Vs
7	VII	$S_1S_2S_3$	$S_1S_2S_3D_4$	+7Vs
8	VIII	S_4	$S_4D_3D_2D_1$	+8Vs
9	IX	S_1S_4	$S_4D_3D_2S_1$	+9Vs
10	X	S_2S_4	$S_4D_3S_2D_1$	+10Vs
11	XI	$S_1S_2S_4$	$S_4D_3S_2S_1$	+11Vs
12	XII	S_3S_4	$S_4S_3D_2D_1$	+12Vs
13	XIII	$S_1S_3S_4$	$S_3D_2D_1D_4$	+13Vs
14	XIV	$S_2S_3S_4$	$S_4S_3S_2D_1$	+14Vs
15	XV	$S_1S_2S_3S_4$	$S_1S_2S_3S_4$	+15Vs
16	XVI	Nil	Nil	0

TABLE 1 switching sequence

Comparison of the Proposed Topology with the Other Topology

The modified hybrid multilevel inverter involves only eight number of switches compare to the conventional hybrid multilevel inverter. In the conventional hybrid multilevel; inverter involves the 16 number of switches, but the table 2 shows each stage is similar to the different multilevel inverter topology. Therefore the proposed modified hybrid multilevel inverter has less switching losses, simple control circuit and less complexity than the conventional multilevel inverter.

Inverter topology	11-level inverter proposed in [15]	15-level Inverter proposed in [6]	15-level Inverter proposed in [7]	31-level Proposed inverter
Main switches	11	16	10	8
Diodes	0	0	1	4
Total	11	16	11	12

TABLE 2 Switch requirement

Simulation Results

This section deals with the simulation validation of the proposed multilevel inverter topology. For the proposed asymmetric multilevel inverter only the simulation results are presented, but both single phase and three phase simulation results are given.

For the single phase system the load is R-load and for the three system RL load(three phase induction motor)

A *Asymmetric topology*

For the asymmetric topology, firstly a design example of the proposed multilevel inverter is given and then it is used for simulation studies.

A1 Design example

The aim is to design a three phase, 400V multilevel inverter with minimum 31-levels of output voltage.

Therefore, a 31-level 400V voltage waveform based on the proposed multilevel inverter topology is shown in Fig 3 & 4 for both single phase as well as three phase system. The proposed 31-level inverter use 8 IGBT switches, 4 power diodes and 4 asymmetric DC voltage source. The proposed inverter is used to fed three phase induction motor and the performance is studied . since the proposed inverter can be used for induction drive speed control.

A2 SIMULATION STUDIES

The validity of the proposed multilevel inverter is demonstrated with the help of simulation results using MATLAB/SIMULINK software.

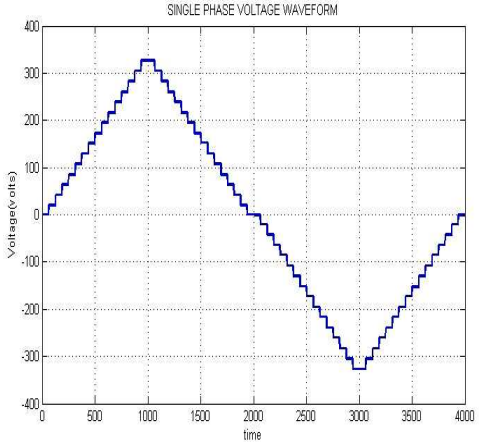

Fig 4 single-phase output voltage

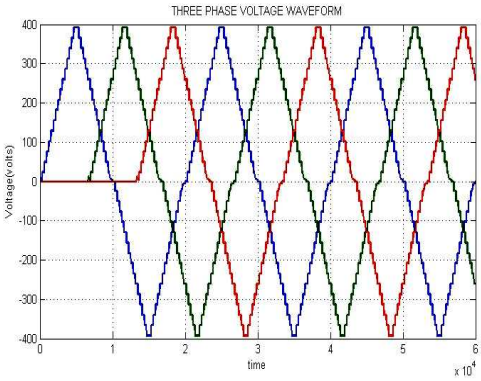

Fig 5 Three-phase voltage waveform

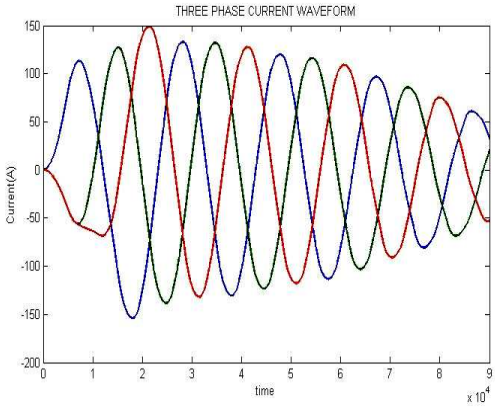

Fig 6 Three phase current waveform

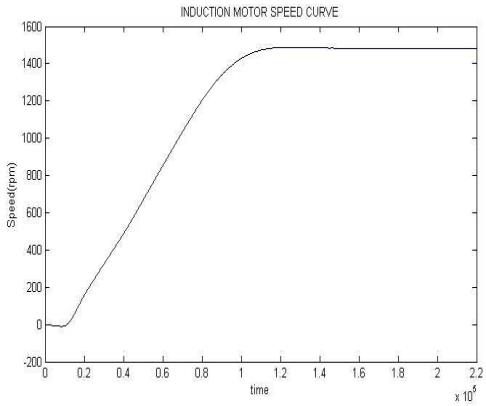

Fig 7 Proposed inverter fed Induction motor speed curve

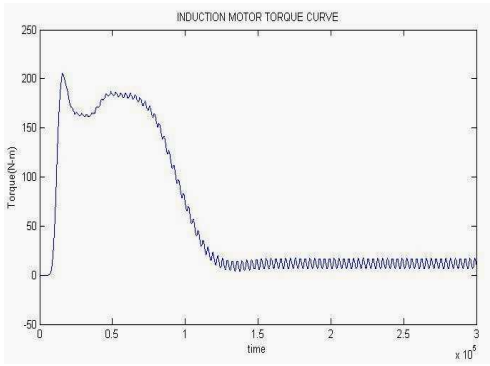

Fig 7 Proposed inverter fed Induction torque curve

The output voltage of each stage is shown in fig 4 clearly the output voltage of each inverter stage corresponds to its dc voltage source. Considering the figure 2(b), the first stage of the inverter operate with high switching frequency and the last stage of the inverter operates with highest voltage and low switching frequency. The switching frequency of the switches S_1-S_4 is 1600Hz, 800Hz, 400Hz, 200Hz, respectively. The output voltage of the main inverter is non-negative. The polarity of the voltage is changed using the H-bride connected to the output of the main inverter.

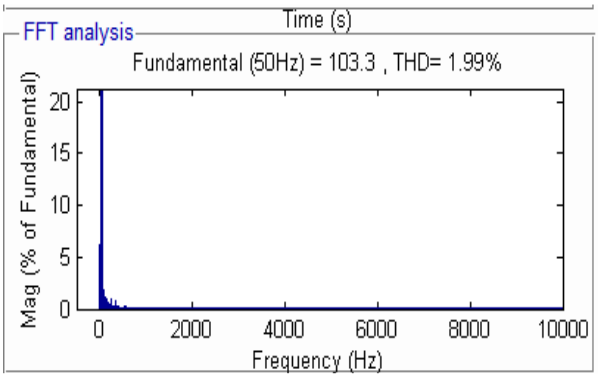

Fig 8 THD waveform

The THD is around 1.99% this figure 8 shows a good correspondence with the simulation results.

Conclusion

In this paper, a new topology of hybrid multilevel inverter has been proposed. The optimal structure for the proposed multilevel inverter were obtained considering several factors such as the number of switching devices, number of dc voltage source, number of output voltage levels, total harmonic distortion etc., The comparison between the conventional H-bridge inverter and the proposed multilevel inverter were done and found the switching loss are get reduced. The simulation results for proposed 31-level inverter are done by conducting simulation studies on a induction motor drive**.**

TABLE II Key parameters of the proposed inverter

SOURCE	VOLTAGE
V_{dc1}	26.5V
V_{dc2}	52.5V
V_{dc3}	105V
V_{dc4}	210V

TABLE III Key parameter of the induction motor
Induction motor

Parameters	Values
Induction motor	3HP, 50 Hz,
Stator resistance	Rs=0.435 ohms
Rotor resistance	Rr=0.816 ohms

Reference

[1] L.G.Franquelo et.al ., "The age of multilevel converters arrives", IEEE Industrial Electronics Magazine",vol.2,no.2,pp 28-39,June 2008

[2] J.Rodriguez,J.S.Lai, and F.Z.Peng, "Multilevel inverters: Survey of topologies ,controls, and applications",IEEE Trans. Ind .Appl.,vol.49,no.4,pp.724-738,Aug 2002

[3] Z.Du, L.m.Tolbert, J.N.Chiasson, and B.Opineci, "A cascaded multilevel inverter using a single dc power source", in Proc. IEEE APEC,2006,pp.426-430.

[4] Fang Zheng Peng "A Generalized Multilevel InverterTopology with Self Voltage Balancing", IEEE Trans. Ind .Appl.,vol.37,no.2,March/April 2001

[5] Ebrahim Babaei "A Cascaded Multilevel converter Topology With Reduced Number of Switches", IEEE Trans. Power Electron vol.23,no.6,Nov 2008

[6] Javad Ebrahimi, Student Member, IEEE, Ebrahim Babaei, Member, IEEE,and Goverg B. Gharehpetian, Senior Member, IEEE " A New Topology of Cascaded Multilevel Converters With Reduced Number of Components for High-Voltage Applications", ieee transactions on power electronics, vol. 26, no. 11, November 2011.

[7] S. Ramkumar, V. Kamaraj, S. Thamizharasan, ''A new series parallel switched multilevel dc-link inverter topology'', ELSEVIER, Electrical Power and Energy Systems 36 (2012) 93–99.

[8] A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Dou-ble flying capacitor multicell converter based on modified phase-shifted pulsewidth modulation," IEEE Trans. Power Electron., vol. 25, no. 6,pp. 1517–1526, Jun. 2010.

[9] S. Vazquez, J. I. Leon, L. G. Franquelo, J. J. Padilla, and J. M. Carrasco, "DC-voltage-ratio control strategy for multilevel cascaded converters fedwith a single DC source," IEEE Trans. Ind. Electron., vol. 56, no. 7, pp. 2513–2521, Jul. 2009.

[10] Z. Du, L. M. Tolbert, J. N. Chiasson, and B. Ozpineci, "A cascade mul-tilevel inverter using a single dc source," in Proc. Appl. Power Electron. Conf. Expo., 2006, pp. 426–430.

[11] E. Babaei, "A cascade multilevel converter topology with reduced number of switches,"IEEE Trans. Power Electron, vol. 23, no. 6, pp. 2657–2664, Nov. 2008.

[12] E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topol-ogy with minimum number of switches," Elsevier J. Energy Convers. Manage., vol. 50, no. 11, pp. 2761–2767, Nov. 2009.

[13] R. Marquardt, "Modular multilevel converter: An universal concept for HVDC-Networks and extended DC-Bus-applications," inProc. Int. Power Electron. Conf., 2010, Jun. 2010.

[14] Rokan Ali Ahmed, S. Mekhilef, Hew Wooi Ping, ''New multilevel inverter topology with reduced number of switches'',Proceedings of the 14th International Middle East Power Systems Conference (MEPCON'10), Cairo University, Egypt, December 19-21, 2010, Paper ID 236.